

CS-00-122



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July 12, 2001

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
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Subject:

Serial No. 09/838,513 04/20/01

Shaoyin Chen, Ze Xiang Shen,
Alex See, Lap Chan

A NOVEL METHOD TO FORM C54 TiSi₂
FOR IC DEVICE FABRICATION

Grp. Art Unit:

RECEIVED

JUL 20 2001

TC 2200 MAIL ROOM

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,937,325 to Ishida, "Formation of Low
Resistivity Titanium Silicide Gates in Semiconductor Integrated
Circuits", teaches using laser annealing to form C49 TiSi₂,
then a rapid thermal annealing (RTA) to form C54 TiSi₂ on a
polysilicon gate.

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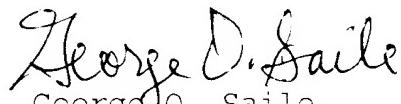


U.S. Patent 6,054,387 to Fukuda, "Method for Forming a Silicide Region", teaches forming C49 TiSi₂ by RTA, then warping the device while performing a second RTA to form C54 TiSi₂.

U.S. Patent 6,071,552 to Ku, "Insitu Formation of TiSi₂/TiN Bi-Layer Structures Using Self-Aligned Nitridation Treatment on Underlying CVD-TiSi₂ Layer", discloses deposition of C49 TiSi₂, then an RTA to form C54 TiSi₂.

U.S. Patent 5,956,137 to Lim et al., "In-Line Process Monitoring Using Micro-Raman Spectroscopy", discloses a method to use Raman analysis to determine the phase of a silicide.

Sincerely,


George D. Saile
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